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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER | |
|---|---|
| LEVIN, NAUM B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/064,444 | HABITZ, PETER A. | |
| | Examiner | Art Unit | |
| | Naum B Levin | 2825 | |

*-- Th MAILING DATE of this communication appears on th cov r sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 and 12-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Raghavan et al. (US Patent 5,896,300).

Raghavan discloses methods, apparatus and computer program products for performing post-layout verification of microelectronic circuitry including:

(1), (12) A method and program storage device for extracting circuit characteristics from a circuit design, said method comprising (col.9, ll.28-37):

extracting first cell (electrical) characteristics from a portion of said circuit design using a first set of environmental conditions (worst case delay model/maximum delay model) (col.3, ll.45-67 and col.4, ll.1-5);

extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions (best delay model/minimum delay model) (col.3, ll.45-67 and col.4, ll.1-5);

determining a difference between said first cell characteristics and said second cell characteristics (col.4, ll.6-22); and

labeling a placeability of said portion of said circuit design based on said difference (identifying timing critical paths/timing errors) (col.5, ll.8-33);

(2), (7), (13) The method and program storage device, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance (col.3, ll.45-67 and col.4, ll.1-5);

(3), (8), (14) The method and program storage device, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment (col.3, ll.55-59);

(4), (9), (15) The method and program storage device, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit (col.4, ll.16-18);

(5), (10), (16) The method and program storage device, wherein said labeling of said placeability comprises:

comparing (filtering) said difference to (against) a predetermined standard/error tolerance (col.4, ll.23-25 and col.11, ll.24-27); and

labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard/within the error tolerance (col.4, ll.25-27; col.3, ll.45-67; col.11, ll.46-67 and col.12, ll.1-4 and ll.34-40);

(6) A method of extracting circuit characteristics from a circuit design, said method comprising:

extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions (col.3, ll.45-67 and col.4, ll.1-5);

extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions (col.3, ll.45-67 and col.4, ll.1-5);

determining a difference between said first cell characteristics and said second cell characteristics (col.4, ll.6-22);

labeling a placeability of said portion of said circuit design based on said difference (col.5, ll.8-33); and

replacing (correcting and changing layout/simulation) said portion of said circuit with a placeholder cell if said portion of said circuit design is freely placeable (col.7, ll.56-67; col.8, ll.1-10 and Figs. 5 and 7, position 16E).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan in view of Darden et al. (US Patent 6,185,722).

4. With respect to claim 11 Raghavan teaches the features above but lacks a method of extracting circuit characteristics from the circuit design further comprising calculating average cell characteristics from portion of said circuit design for said placeholder cell based on an average environment.

Darden discloses three dimensional track-based parasitic extraction Including:

(11) The method in claim 6, further comprising calculating average cell characteristics from said portion of said circuit design for said placeholder cell based on an average environment/nominal case/search 2 (col.4, ll.1-20 and col.8, ll.16-37).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Darden's teaching regarding the method of extracting circuit characteristics from the circuit design further comprising calculating average cell characteristics from portion of said circuit design for said placeholder cell based on an average environment and use it in Raghavan's invention to improve accuracy of the integrated circuit design.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan in view of Darden, and further in view of Chang et al. (US Patent 5,901,063).

6. With respect to claims 17-21 Raghavan and Darden teach the features above but lacks a method of extracting circuit characteristics from the circuit design further comprising simplifying said placeholder cell in a process comprising: shorting all conductors in said portion of said circuit design to a ground node; merging all

conductors in a given level of said portion of said circuit design; removing all conductors that are covered by overlying conductors from said portion of said circuit design; and merging conductors outside said portion of said circuit design that are within a predetermined distance to said circuit design with conductors within said portion of said circuit design.

Chang discloses system and method for extracting parasitic impedance from Integrated circuit layout including:

(17) A method of extracting circuit characteristics from a circuit design, said method further including:

simplifying said placeholder cell in a process comprising:

shorting all conductors in said portion of said circuit design to a ground node (col.9, ll.45-67; col.10, ll.1-13);

merging/combining/grouping all conductors in a given level of said portion of said circuit design (col.7, ll.8-27; col.9, ll.45-67; col.10, ll.1-13);

removing all conductors that are covered by overlying/overlapping conductors from said portion of said circuit design (col.3, ll.61-67; col.4, ll.1-9); and

merging conductors outside said portion of said circuit design that are within a predetermined distance to said circuit design with conductors within said portion of said circuit design (col.7, ll.28-46; col.10, ll.43-50; col.12, ll.35-39 and ll.45-67; col.10, ll.1-24; col.16, ll.63-67 and col.17, ll.1-6).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Changs's teaching regarding the method of extracting

circuit characteristics from the circuit design further comprising simplifying said placeholder cell in a process comprising: shorting all conductors in said portion of said circuit design to a ground node; merging all conductors in a given level of said portion of said circuit design; removing all conductors that are covered by overlying conductors from said portion of said circuit design; and merging conductors outside said portion of said circuit design that are within a predetermined distance to said circuit design with conductors within said portion of said circuit design and use it in Raghavan's and Darden's inventions to further improve accuracy and efficiency of the circuit design.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Djaja et al. (US Patent 5,359,535) discloses method that comprises selecting a logic gate, and constructing a model which predicts the delay time of the logic gate. The predetermined target delay time is typically a minimum delay time, but may also be a requirement for matching the delay time of another signal path or a constraint such as a falling between a maximum delay time and a minimum delay time.

Dewey, III et al. (US Patent 6,473,887) teaches method and structure for performing capacitance extraction during the design of an integrated circuit that includes adding a virtual wires to the integrated circuit , wherein said virtual wires are alternatively connected to ground and noise signals to extract capacitance from said circuit under differing conditions.

DeCamp et al. (US Patent 5,761,080) describes the method for calculating the

parasitic capacitance in a semiconductor device using technology data file which includes such parameters as metal layer thickness and the distances between metal layers. The tolerances for these parameters can also be included, and thus the file could also include nominal, best and worst case dimensions.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 703-305-0144. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER

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